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TITLE OF THE INVENTION:

MOLD DIE AND METHOD FOR MANUFACTURING SEMICONDUCTOR DEVICE USING THE SAME

BACKGROUND OF THE INVENTION:

~~(Field of the Invention)~~

The present invention relates to a mold die and method ~~for manufacturing~~ of manufacture of a semiconductor device using ~~it, in particular~~ the mold die; and, more particularly, the invention relates to a technology ~~that can effectively apply to~~ in which is used effectively a die for sealing ~~by transfer mold~~ which is mounted a semiconductor chip ~~borne~~ on a wiring board via an elastic material and an opening of the wiring board by transfer mold processing.

~~(Prior Art)~~

As an example of ~~the~~ conventional semiconductor devices known in a form referred to as a BGA (Ball Grid Array) ~~is a semiconductor device which~~ includes a semiconductor chip, an interposer (wiring board) having an insulating substrate on which a conductive pattern is provided, and an elastic material (elastomer) disposed therebetween for providing stress relaxation. The semiconductor device ~~is~~ hereafter referred to ~~a semiconductor device that~~ includes the above-described elastic material, unless otherwise specified.

The above-described semiconductor device includes, for example, as shown in Figure 9, an opening 4 ~~on~~ in the interposer which includes an ~~having the above-described~~ insulating substrate 101 on which the conductive pattern 102 is provided, and ~~on~~ on the ~~above-described~~ elastic material 2. The ~~above-described~~ conductive pattern 102 and an external electrode 301 of the ~~above-described~~ semiconductor chip 3 are electrically connected ~~over~~ by way of the

~~above-described~~ opening 4.

In addition to the ~~above-described~~ opening 4, the ~~above-described~~ insulating substrate 101 also includes an opening (not shown) for forming an external connecting terminal 6. The opening 4 over which the ~~above-described~~ conductive pattern 102 and the external electrode 301 of the semiconductor chip 3 are connected is hereafter referred to as a bonding opening. The opening for forming the ~~above-described~~ external connecting terminal 6 is hereafter referred to as an external terminal opening.

In the above-described semiconductor device, an insulating resin 5 seals the periphery of the ~~above-described~~ semiconductor chip 3, for example, as shown in Figure 9. The ~~above-described~~ insulating resin 5 also seals the ~~above-described~~ bonding opening 4.

The periphery of the ~~above-described~~ semiconductor chip 3 and the ~~above-described~~ bonding opening 4 may be sealed, for example, by transfer mold processing.

The above-described transfer mold processing is carried out by, for example, as shown in Figure 10, sandwiching the interposer (insulating substrate 101) bearing the ~~above-described~~ semiconductor chip 3 between a first die (hereafter referred to as a top die) 7 having a recess 7A in a predetermined form and a second flat die (hereafter referred to as a bottom die) 8, by causing the insulating resin 5 to flow into the resulting space formed therebetween, and by curing the resin 5 (see for example Japanese application patent laid-open publication No. 2002-353361).

Semiconductor devices in a similar form to the above-described

semiconductor device include a semiconductor device in which ~~that electrically connects~~ the ~~above-described~~ conductive pattern 102 and the external electrode 301 of the ~~above-described~~ semiconductor chip 3 are electrically connected via a bonding wire.

The ~~above-described~~ semiconductor device using ~~the~~ a bonding wire may be transfer molded using ~~with~~ a groove (recess) provided on a portion overlapping the ~~above-described~~ bonding opening 4 of the ~~above-described~~ interposer to ensure the sealing of the loop of the ~~above-described~~ bonding wire (see for example Japanese application patent laid-open publication No. 2000-058711 (Figure 6)).

SUMMARY OF THE INVENTION:

In the above-described conventional technologies, however, the ~~above-described~~ bottom die 8 has a flat surface 8A which is brought into contact with the ~~above-described~~ insulating substrate 101. Thus, any bending ~~Any winding~~ or distortion of the ~~above-described~~ insulating substrate 101 may ~~thus~~ cause a space to appear between the ~~above-described~~ bottom die 8 and the ~~above-described~~ insulating substrate 101, which is sandwiched between the ~~above-described~~ top die 7 and bottom die 8, as shown in Figure 11.

In particular, each opening of the ~~above-described~~ insulating substrate 101, which is generally formed by stamping with a die, may ~~thus~~ often cause bending ~~winding~~ or distortion around the opening. The ~~above-described~~ bonding opening 4 may also be subjected to ~~receive~~ a load caused by ~~the~~ electrical connection of the ~~above-described~~ conductive pattern 102 and the external electrode 301 of the ~~above-described~~ semiconductor chip 3.

Thus, bending or distortion often occurs around the
~~The above-described~~ bonding opening 4 ~~may thus often cause winding or distortion around it~~.

With any ~~winding~~ bending or distortion generated around the ~~above-described~~ bonding opening 4, the transfer mold may allow the insulating resin 5 ~~flowed~~ which flows into the ~~above-described~~ bonding opening 4 to leak into the space ~~between~~ formed between the ~~above-described~~ bottom die 8 and the ~~above-described~~ insulating substrate 101, as shown in Figure 11.

~~Any~~ The thin insulating substrate 101 cannot bear the injection pressure from the flow of the ~~above-described~~ insulating resin 5 and may float. As a result, the ~~above-described~~ insulating resin 5 may spread over the surface of the ~~above-described~~ insulating substrate 101, as shown in Figure 12.

The ~~above-described~~ insulating substrate 101 includes, for example, as shown in Figure 12, ~~the above-described~~ external terminal openings 101A outside the ~~above-described~~ bonding opening 4. Thus, if the insulating resin 5 which flows into the ~~above-described~~ bonding opening 4 during the ~~above-described~~ transfer mold operation leaks out, the front end 5A of the ~~above-described~~ leaked insulating resin 5 may spread over the area of the ~~above-described~~ external terminal openings 101A and flow into the ~~above-described~~ external terminal openings 101A.

The ~~above-described~~ insulating resin 5 which flows into the ~~above-described~~ external terminal openings 101A may cause poor electrical conduction between the ~~above-described~~ external connecting terminal 6 ~~formed~~ and the ~~above-described~~ conductive pattern 102.

In particular, recent semiconductor devices, which tend to be

smaller and to be ~~in~~ provided with a higher density, ~~have~~ are characterized by a smaller distance between the ~~above-described~~ bonding opening 4 and the ~~above-described~~ external terminal openings 101A. The ~~above-described~~ external terminal openings 101A also tend to have a smaller area. ~~The above-described~~ Thus, the leaked insulating resin may ~~thus~~ more readily cause ~~the~~ poor electrical conduction.

As described above, there has been a problem with the conventional method ~~by~~ using transfer mold processing for manufacturing the above-described semiconductor device in that the ~~above-described~~ semiconductor devices may have a reduced manufacturing yield.

Accordingly, an object of the present invention is to provide a ~~technology that can~~ technique with which it is possible to prevent leakage seal the opening of the interposer during ~~by~~ transfer mold processing ~~with the leak~~ of the insulating resin from the ~~above-described~~ opening ~~prevented~~, thereby improving the manufacturing yield of the semiconductor devices.

These and other objects and novel features of the present invention will become apparent upon review of the following description in ~~of~~ this specification and the accompanying drawings.

The present invention as disclosed in this application will be summarized as follows.

(1) A mold die ~~comprising~~ includes a first die having a recess in a predetermined form and a second flat die, the ~~above-described mold die being for disposing the above-described~~ being disposed first die on a surface of a wiring board which has a plurality of openings ~~and~~, which surface bears a semiconductor chip ~~tip~~ via an elastic material, ~~which surface bears the above-described~~

semiconductor chip, and for disposing the above-described second die is disposed on a back of the above-described surface of the above-described wiring board opposite to the surface which bears the above-described semiconductor chip. The molding die is used for sealing, with an insulating resin, a periphery of the above-described semiconductor chip and at least one of the above-described openings of in the above-described wiring board, wherein the above-described second die comprises a protrusion disposed around an area overlapping the above-described opening which is sealed with the above-described insulating resin.

According to the above-described Example (1) means, when the above-described first die and the above-described second die sandwich the above-described wiring board, the above-described protrusion on the above-described second die can press against and apply pressure to the above-described wiring board (insulating substrate). With the above-described protrusion pressing against the above-described wiring board, the above-described elastic material can deform which attempts and exert a force to return to its original shape.

The above-described wiring board (insulating substrate) may then receive from the above-described elastic material a force opposite to the force applied from the above-described protrusion of the above-described second die. PA Higher degree of contact can thus be provided between the above-described second die and the above-described wiring board (insulating substrate), thereby preventing the insulating resin which flows into the above-described opening from leaking in between the above-described wiring board (insulating substrate) and the above-described second die.

(2) A method of manufacture of for manufacturing a semiconductor device by sealing,

by transfer mold using a die, a semiconductor chip borne on a wiring board via an elastic material, which board includes an insulating substrate with a plurality of openings thereon on which a conductive pattern is formed, and by sealing at least one of the above-described openings, wherein a die having a protrusion around an area overlapping the above-described sealed opening is used for a back of the surface of the above-described wiring board which bears the above-described semiconductor chip.

The above-described (2) means is a method for manufacturing a semiconductor device using the above-described (1) means. Use of the mold die of the above-described (1) means can prevent the insulating resin flowed into the above-described opening from leaking out and flowing into an opening not sealed by the above-described insulating resin. It is thus possible to improve the manufacturing yield of the above-described semiconductor device.

In the following, the present invention as well as its embodiments (examples) will be described in more detail with reference to the accompanying drawings.

Like reference characters indicate the functionally identical elements throughout all the illustrative drawings of the examples, and the repeated description is omitted.

BRIEF DESCRIPTION OF THE DRAWINGS:

Figure 1 shows a plan diagram of the schematic configuration of the semiconductor device according to the present invention.

Figure 2 ~~shows a diagram of the schematic configuration of the semiconductor device according to the present invention, which~~ is a cross-sectional view taken along line A - A' in Figure 1.

Figure 3 ~~shows~~ is a diagram of the ~~schematic~~ configuration of ~~the~~ a mold die in an example according to the present invention.

Figure 4 ~~shows a diagram of the schematic configuration of the mold die in the example, which~~ is an enlarged cross-sectional view of ~~the~~ a characteristic part of the mold die shown in Figure 3.

Figure 5 ~~shows~~ is a ~~illustrative~~ cross-sectional diagram ~~of~~ illustrating the operational advantage of the mold die ~~in the example, which is a cross-sectional view of the condition~~ during the molding process ~~mold~~.

Figure 6 ~~shows~~ is a ~~illustrative~~ cross-sectional diagram ~~of~~ illustrating the operational advantage of the mold die ~~in the example, which is a cross-sectional view of the semiconductor device~~ after the molding process ~~mold~~.

Figure 7 shows a ~~illustrative cross-sectional diagram~~ back view of the semiconductor device illustrating ~~of~~ the operational advantage of the mold die ~~in the example, which is a back view of the semiconductor device~~ after the molding process ~~mold~~.

Figure 8 ~~shows~~ is a cross-sectional diagram illustrating an application of ~~the~~ an ~~above-described~~ example of the mold die.

Figure 9 ~~shows~~ is a cross-sectional diagram ~~of an example of the schematic configuration~~ of a conventional BGA type semiconductor device.

Figure 10 ~~shows~~ is a cross-sectional diagram ~~of the schematic configuration~~ of a conventional mold die.

Figure 11 ~~shows~~ is a ~~illustrative~~ diagram illustrating ~~of~~ the problems of the

conventional mold die.

Figure 12 shows a [illegible] diagram of the problems of the conventional mold die.

DESCRIPTION OF THE INVENTION:

Before describing the examples of the present invention, the schematic configuration of the semiconductor device according to the present invention will be described.

Figures 1 and 2 show diagrams of the schematic configuration of the semiconductor device according to the present invention. Figure 1 shows a plan view of the semiconductor device. Figure 2 shows a cross-sectional view taken along line A - A' in Figure 1.

The semiconductor device according to the present invention includes an interposer (wiring board) having an insulating substrate 101 on which a conductive pattern 102 is provided, and a semiconductor chip 3 bonded on the above-described interposer via an elastic material (elastomer) 2, as shown in Figures 1 and 2.

The conductive pattern 102 of the above-described interposer and the external electrode 301 of the above-described semiconductor chip 3 are electrically connected over the opening 4 provided on the above-described interposer (insulating substrate 101) and elastic material 2, as shown in Figure 2. The above-described opening 4 is hereafter referred to as a bonding opening.

In the above-described semiconductor device, an insulating resin 5 seals the periphery of the above-described semiconductor chip 3, as

shown in Figure 2. The ~~above-described~~ insulating resin 5 also seals the ~~above-described~~ bonding opening 4.

The ~~above-described~~ conductive pattern 102 of the interposer is provided, for example, as shown in Figure 2, on the surface where the ~~above-described~~ semiconductor chip 3 is bonded. The ~~above-described~~ conductive pattern 102 includes, for example, terminals for connection to a print wiring board, such as those referred to as a motherboard and a daughter board.

The ~~above-described~~ insulating substrate 101 of the interposer includes openings in the regions of the ~~above-described~~ terminals. The openings include external connecting terminals 6 of a ball-like shaped bonding agent. The opening for providing the ~~above-described~~ external connecting terminal 6 is hereafter referred to as an external terminal opening.

The ~~above-described~~ elastic material 2 is, for example, PTFE (poly-tetrafluoroethylene). The ~~above-described~~ elastic material 2 has a thickness of, for example, about 150 μm.

The ~~above-described~~ semiconductor device can be manufactured by bonding the ~~above-described~~ semiconductor chip 3 on the ~~above-described~~ interposer via the ~~above-described~~ elastic material 2, followed by electrically connecting the ~~above-described~~ conductive pattern 102 of the interposer and the ~~above-described~~ external electrode 301 of the semiconductor chip 3.

The insulating resin 5 then seals, by transfer mold, the periphery of the ~~above-described~~ semiconductor chip 3 and the ~~above-described~~

bonding opening 4. The ~~above-described~~ external connecting terminal 6 is then formed in the ~~above-described~~ external terminal opening.

Examples will be described below of the configuration of the die (hereafter referred to as a mold die) for use in the above-described transfer mold.

(Example 1)

Figures 3 and 4 ~~show~~ and diagrams of the ~~schematic~~ configuration of the mold die ~~is~~ representing an example according to the present invention. Figure 3 ~~shows~~ is a cross-sectional view of the entire configuration of the mold die. Figure 4 ~~shows~~ is an enlarged cross-sectional view of ~~the~~ a characteristic part of the mold die.

The mold die in ~~the~~ this example includes a pair of a top die 7 and a bottom die 8 ~~sandwiching~~ which sandwich the interposer bearing the ~~above-described~~ semiconductor chip 3, as shown in Figure 3. The ~~above-described~~ top die 7 includes a recess space 7A into which the insulating resin flows for sealing the periphery of the ~~above-described~~ semiconductor chip 3.

The ~~above-described~~ bottom die 8 includes a protrusion 8B in a predetermined form on the upper surface ~~to be~~ so as to come into close contact with the ~~above-described~~ insulating substrate 101 (hereafter referred to as a reference contact surface), as shown in Figures 3 and 4. The ~~above-described~~ protrusion 8B is provided in the form of a loop around a rectangular opening, such as the ~~above-described~~ bonding opening, to be sealed with ~~the above-described~~ insulating resin 5.

The ~~above-described~~ protrusion 8B has such a width that, for example, the above-described protrusion 8B can come into contact with the ~~above-~~

described insulating substrate 101 between the above-described opening 4 and the above-described opening 101A for forming the external connecting terminal, as shown in Figure 4. The above-described protrusion 8B has a height of, for example, about 10μm.

Figures 5 to 7 show illustrative cross-sectional diagrams of the operational advantage of the mold die in the example 1. Figure 5 shows a cross-sectional view of the condition during the mold. Figure 6 shows a cross-sectional view of the semiconductor device after the mold. Figure 7 shows a back view of the semiconductor device after the mold. Figure 5 shows the same cross section as in Figure 4, although it omits the hatching (parallel oblique lines) representing the cross section. Figure 7 is a view from the back of Figure 1.

The mold die in the example 1 can be used for the transfer mold by, as shown in Figure 4, disposing the interposer bearing the above-described semiconductor chip 3 between the top die 7 and the bottom die 8, followed by, for example, sandwiching the above-described insulating substrate 101 between the above-described top die 7 and the above-described bottom die 8, and fastening the substrate 101 with a predetermined pressure.

In the contact portion between the above-described insulating substrate 101 and the above-described protrusion 8B of the bottom die 8, the above-described insulating substrate 101 will be distorted with the force F1 from the above-described protrusion 8B of the bottom die 8. The above-described insulating substrate 101 will have a distorted portion that is pressed by the above-described protrusion 8B of the

bottom die 8, thereby the ~~above-described~~ elastic material 2 also ~~being~~ will be distorted. The ~~above-described~~ elastic material 2 is in a contracted condition and tends to return to ~~the~~ its original condition. Thus, ~~the~~ ~~The above-described~~ insulating substrate 101 ~~may thus~~ will also receive from the ~~above-described~~ elastic material 2 a force F2, which is opposite to the force F1 from the ~~above-described~~ protrusion 8B of the bottom die 8, as shown in Figure 5.

As a result, the degree of contact between the ~~above-described~~ insulating substrate 101 and the ~~above-described~~ protrusion 8B of the bottom die 8 ~~can~~ will be higher than, for example, the degree of contact between the ~~above-described~~ insulating substrate 101 and the ~~above-described~~ reference contact surface 8A of the bottom die 8.

Even ~~with~~ when the ~~above-described~~ insulating substrate 101 ~~having any winding or distortion~~ is distorted in the area around the ~~above-described~~ bonding opening 4, for example, as shown in Figure 11, the ~~above-described~~ protrusion 8B of the bottom die 8 can prevent any space from appearing at the portion where the ~~above-described wiring or~~ distortion occurs.

As described above, the mold die in the example 1 can prevent the insulating resin 5 ~~flowed~~ which flows into the ~~above-described~~ bonding opening 4 from leaking through between the ~~above-described~~ insulating substrate 101 and the ~~above-described~~ bottom die 8.

It is thus possible, for example, as shown in Figures 6 and 7, to prevent ~~the spread~~ any spreading of the front end 5A of the insulating resin 5 ~~flowed~~ which flows into the ~~above-described~~ bonding opening 4, and to prevent the flow of the ~~above-described~~ insulating resin 5 into ~~the~~ an opening 101A for forming the

external connecting terminal.

When the protrusion 8B ~~of~~ on the surface of the ~~above-described~~ bottom die 8 is provided outside the edge of the ~~above-described~~ bonding opening 4, as shown in Figure 4, the insulating resin 5 ~~flowed~~ which flows into the ~~above-described~~ bonding opening 4 can reach the back of the surface of the ~~above-described~~ insulating substrate 101, specifically, the surface on which the ~~above-described~~ semiconductor chip 3 is bonded, so that the front end 5A of the ~~above-described~~ insulating resin 5 can reach outside the edge of the ~~above-described~~ bonding opening 4, as shown in Figures 6 and 7.

As a result, the ~~The~~ interface delamination ~~can~~ will occur less frequently between the ~~above-described~~ insulating substrate 101 and the ~~above-described~~ insulating resin 4 around the above-described bonding opening 4.

As described above, in the mold die ~~in the~~ of example 1 ~~can give~~ a higher degree of contact is produced between the ~~above-described~~ bottom die 8 and the periphery of the bonding opening 4 provided on the interposer, thereby preventing the insulating resin 5 ~~flowed~~ which flows into the ~~above-described~~ bonding opening 4 from leaking in between the ~~above-described~~ insulating substrate 101 and the ~~above-described~~ bottom die 8.

It is thus possible to prevent the insulating resin 5 ~~spread~~ from spreading over the surface of the ~~above-described~~ insulating substrate 101, as shown in Figure 12, and from flowing into the opening 101A for forming the external connecting terminal, thereby improving the manufacturing yield of the semiconductor device.

Figure 8 ~~shows~~ is a cross-sectional diagram ~~of the~~ illustrating an application of the above-described example.

The mold die in ~~the above-described~~ example 1 uses a bottom die 8 on which the area inside the ~~above-described~~ protrusion 8B is approximately the same height as the ~~above-described~~ reference surface 8A, as shown in Figure 3. Additionally, the area inside the ~~above-described~~ protrusion 8B may include a recess 8C, as shown in Figure 8. The ~~above-described~~ recess 8C may have a depth of about 70 μm from the ~~above-described~~ reference surface 8A.

The bottom die 8 with the ~~above-described~~ recess 8C can also include, around the ~~above-described~~ recess 8C, the protrusion 8B with a height of about 10 μm from the ~~above-described~~ reference surface 8A to give higher degree of contact between the ~~above-described~~ bottom die 8 and the insulating substrate 101 around the periphery of the ~~above-described~~ bonding opening 4.

It is thus possible to prevent the insulating resin 5 ~~flowed~~ which flows into the ~~above-described~~ bonding opening 4 from leaking in between the ~~above-described~~ interposer (insulating substrate 101) and the ~~above-described~~ bottom die 8.

When the ~~above-described~~ recess 8C is provided, the insulating resin 5 ~~flowed~~ which flows into the ~~above-described~~ bonding opening 4 may run into the ~~above-described~~ recess 8C. The ~~above-described~~ insulating resin 5 in the ~~above-described~~ recess 8C may be cured to provide the complete semiconductor device in which the ~~above-described~~ cured insulating resin 5 may have ~~the~~ a front end 5A, as shown in Figure 6, of ~~more~~ greater thickness than in the above-described example.

With the bottom die 8 ~~shown~~ as in the above-described example, the

edge of the ~~above-described~~ bonding opening 4 may contact ~~with~~ the reference surface 8A of the ~~above-described~~ bottom die 8, so that the front end 5A of the ~~above-described~~ insulating resin 5 may have ~~varied~~ various shapes.

On the other hand, with the bottom die 8 shown in Figure 8, the base of the ~~above-described~~ recess 8C is lower than the ~~above-described~~ reference surface 8A to prevent the edge of the ~~above-described~~ bonding opening 4 from contacting ~~with~~ the ~~above-described~~ bottom die 8. The front end 5A of the ~~above-described~~ insulating resin 5 can thus have less varied shapes (thicknesses), and the interface delamination ~~can~~ will occur much less frequently between the ~~above-described~~ insulating substrate 101 and the ~~above-described~~ insulating resin 5.

The above-described example 1 ~~describes as~~ provides an illustration of a semiconductor device in which the ~~above-described~~ conductive pattern 102 is deformed to be electrically connected with the ~~above-described~~ external electrode 301 of the semiconductor chip 3. Additionally, the semiconductor device may be one in which, for example, the ~~above-described~~ conductive pattern 102 is connected with the ~~above-described~~ external electrode 301 of the semiconductor chip 3 via a bonding wire.

In this case, to ensure the sealing of the ~~above-described~~ bonding wire, the bottom die with the ~~above-described~~ recess 8C, as shown in connection with Figure 8, may preferably be used rather than the bottom die 8 described in ~~the above-described~~ example 1.

While the present invention has been ~~illustrated above according to~~ described with reference to an ~~the above-described~~ example, it should be understood that the invention

is not limited to the above-described example and various modifications are possible without departing from the spirit thereof.

Representative examples of the invention disclosed in this specification can provide such effects as briefly described as follows.

The opening of the interposer can be sealed by transfer mold processing while preventing leakage of the insulating resin from the ~~above-described~~ opening ~~prevented~~ and ~~with~~ reducing poor electrical conduction of the external connecting terminal due to leakage of ~~the leaked~~ insulating resin ~~reduced~~. It is thus possible to improve the manufacturing yield of the semiconductor device.